WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor wafer, comprising:

cleaning a surface of the wafer during a first time period; and

forming a layer over the surface during a second time period, wherein the first time period includes a cleaning delay period prior to a cleaning portion of the first time period, the cleaning delay period configured such that an end time of the first time period substantially coincides with a start time of the second time period.

2. The method of claim 1 wherein the first time period further includes a loading period and an unloading period.

3. The method of claim 1 wherein the cleaning delay period is a first cleaning delay period and further comprising:

cleaning the layer during a third time period; and

forming a conductive material over the layer during a fourth time period, wherein the third time period includes a second cleaning delay period prior to a cleaning portion of the third time period, the second cleaning delay period configured such that a third time period end time substantially coincides with a fourth time period start time.

4. A method of manufacturing semiconductor device gate dielectrics, comprising:

cleaning a first substrate surface during a first time period;

forming a first insulating layer over the first substrate surface during a second time period subsequent to the first time period;

cleaning a second substrate surface during a third time period; and

forming a second insulating layer over the second substrate surface during a fourth time period subsequent to the second and third time periods, wherein the third time period includes a cleaning delay period prior to a cleaning portion of the third time period, the cleaning delay period configured such that an end time of the third time period substantially coincides with a start time of the fourth time period.

5. The method of claim 4 wherein cleaning the second substrate during the third period includes:

configuring the second substrate surface in a process chamber prior to the cleaning delay period;

exposing the second substrate surface to a cleanser in the process chamber after the delay period; and

removing the second substrate surface from the process chamber after exposing the second substrate surface to the cleanser.

6. The method of claim 4 wherein cleaning the second substrate during the third period includes:

configuring the second substrate surface in a process chamber after the cleaning delay period;

exposing the second substrate surface to a cleanser in the process chamber after configuring the second substrate surface in the process chamber; and

removing the second substrate surface from the process chamber after exposing the second substrate surface to the cleanser.

7. The method of claim 4 wherein the first and second substrate surfaces are individually cleaned in a common process chamber.

8. The method of claim 4 wherein the first and second insulating layers are individually formed in a common process chamber.

9. The method of claim 4 wherein forming the second insulating layer during the fourth time period includes:

configuring the second substrate surface in a process chamber;

exposing the second substrate surface to an oxidizing environment to form an oxide layer; and

removing the second substrate surface from the process chamber.

10. The method of claim 9 wherein the oxidizing environment is a rapid thermal oxidizing environment comprising NO gas and the second insulating layer is a nitrided oxide layer.

11. The method of claim 10 wherein forming the second insulating layer during the fourth time period further includes exposing the nitrided oxide layer to a decoupled plasma nitridation environment.

12. The method of claim 11 wherein forming the second insulating layer during the fourth time period further includes exposing the nitrided oxide layer to a rapid thermal processing environment to anneal the nitrided oxide layer after the exposure to the decoupled plasma nitridation environment.

13. The method of claim 12 wherein the oxidizing environment is a first oxidizing environment and forming the second insulating layer during the fourth time period further includes exposing the nitrided oxide layer to a second oxidizing environment after the exposure to the rapid thermal processing environment.

14. The method of claim 12 wherein forming the second insulating layer during the fourth time period further includes exposing the nitrided oxide layer to a nitrogen-containing annealing environment.

15. The method of claim 4 wherein the first and second insulating layers each have a thickness ranging between about 10 Angstroms and about 20 Angstroms.

16. The method of claim 4 wherein forming the second insulating layer commences within about 30 seconds of the completion of the second substrate surface cleaning.

17. The method of claim 4 wherein cleaning the first and second substrate surfaces includes exposing the first and second substrate surfaces individually to an AM1 chemistry.

18. A system for manufacturing semiconductor device gate dielectrics, comprising:

a cleaner configured to clean a surface of a substrate within a first time period;

a former configured to form a layer over the surface within a second time period exceeding the first time period in duration;

a transporter configured to transport the substrate between the cleaner and the former within a third time period; and

a controller configured to control the cleaner, the former and the transporter and to delay a start time of the first time period such that a duration of the third time period is less than the second time period.

19. The system of claim 18 wherein the duration of the third time period is less than about 30 seconds.

20. The system of claim 18 wherein one of the cleaner and the controller is configured to determine an optimized start time delay of the first time period such that the third time period is a minimized third time period.